



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Bedichek et al.

Examiner:

Makhdoom, Samarina

Serial No. 09/417,447

Art Unit:

2123

Filing Date: December 23, 1999

For:

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MAPPINGS

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Technology Center 2100

Hon. Assistant Commissioner for Patents Washington, D.C. 20231

AMENDMENT AND RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed July 31, 2002, the following amendment and responses to the above captioned patent application are respectfully submitted. Reconsideration of the above captioned patent application is respectfully requested.

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Please add the following new Claim:

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Examiner: Makhdoom, Samarina

Art Unit 2123 TRANS18

15. (New) In a computer which translates instructions from a target instruction set to a host instruction set, a method for determining validity of a translated instruction comprising:

testing a memory address of a target instruction to be executed against a memory address associated with a translation of a target instruction, wherein said translation is linked to a translation of another target instruction;

executing said translation if said memory addresses compare; and generating an exception if said memory addresses do not compare.

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